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EXAMINER	
PETRANEK, JACOB ANDREW	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 04/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/747,625	DEVALE ET AL.	
	Examiner	Art Unit	
	Jacob Petranek	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/7/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-24 are pending.

2. The office acknowledges the following papers:

Oath and IDS filed on 5/7/2004,

POA filed on 9/20/2005.

Priority

3. No claim for priority has been made in this application.

Drawings

4. The Examiner contends that the drawings submitted on 12/30/2003 are acceptable for examination proceedings.

Specification

5. The disclosure is objected to because of the following informalities:

6. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. The Applicant's cooperation is requested in correcting any errors of which the Applicant may become aware.

7. Appropriate correction is required.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1-5, 7-13, 15-21, and 23-24 are rejected under 35 U.S.C. §103(a) as being unpatentable over Kadambi et al. (U.S. 6,934,830), in view of Megiddo et al. (U.S. 6,996,676), further in view of Cherabuddi (U.S. 6,263,416).

10. As per claim 1:

Kadambi disclosed a method, comprising:

A register cache storing physical registers (Kadambi: Figure 1 element 102, column 3 lines 13-33)(A register pane is a smaller storage unit that caches register values.)

Kadambi failed to teach monitoring at least one instruction in an instruction window; tracking one or more physical register references associated with one or more physical registers called on by said at least one instruction; determining a reference count for said one or more physical registers based on said one or more physical register references; determining a potential significance for data of said one or more physical registers based on said reference count; and updating at least one register cache according to said potential significance.

However, Megiddo disclosed tracking one or more physical register references associated with one or more physical registers called on by said at least one instruction (Kadambi: Column 4 lines 40-49)(Megiddo: Column 3 lines 35-46)(The combination of

Kadambi and Megiddo results in the FBR algorithm maintaining a counter for all of the physical registers stored in the register pane.);

Determining a reference count for said one or more physical registers based on said one or more physical register references (Kadambi: Column 4 lines 40-49)(Megiddo: Column 3 lines 35-46)(The combination of Kadambi and Megiddo results in the FBR algorithm maintaining a counter for all of the physical registers stored in the register pane. The reference count can be determined by looking at the counter for the physical register.);

Determining a potential significance for data of said one or more physical registers based on said reference count (Kadambi: Column 4 lines 40-49)(Megiddo: Column 3 lines 35-46)(The combination of Kadambi and Megiddo results in the FBR algorithm maintaining a counter for all of the physical registers stored in the register pane. The significance of the count value is that a higher count value means the register is referenced often and a lower count value means that the register is being referenced infrequently.); and

Updating at least one register cache according to said potential significance (Kadambi: Column 4 lines 40-49)(Megiddo: Column 3 lines 35-46)(The combination of Kadambi and Megiddo results in the FBR algorithm maintaining a counter for all of the physical registers stored in the register pane. The potential significance of having a lower count value will mean that upon a replacement of a physical register within the register pane, the lowest count value will be used for the replacement.).

Kadambi suggests a plurality of replacement algorithms that could be used for

replacing physical registers in the register pane, such as LRU, random, and round robin (Kadambi: Column 4 lines 40-49). The frequency-based replacement (FBR) algorithm has the advantage over the algorithms suggested by Kadambi because it seeks to combine the advantages of a LRU and LFU algorithms. One of ordinary skill in the art would have been motivated to use the FBR algorithm as a cache replacement method for the register pane for the advantage of more accurately replacing registers that won't be used. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the FBR algorithm to replace physical registers in the register pane for the advantage of better replacement performance over the algorithms suggested by Kadambi.

Kadambi and Megiddo failed to teach monitoring at least one instruction in an instruction window;

However, Cherabuddi disclosed Monitoring at least one instruction in an instruction window (Cherabuddi: Figure 5 element 506, column 5 lines 1-11 and 31-54);

The advantage of using a central instruction window is that it allows for instructions to execute out-of-order and execute speculatively, which results in increased processing performance (Cherabuddi: Column 1 lines 13-28). One of ordinary skill in the art would have been motivated to implement a central instruction window for the advantage of increased performance. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement a central instruction window to allow for out-of-order execution and speculative execution to increase performance.

11. As per claim 2:

Kadambi, Megiddo, and Cherabuddi disclosed the method of claim 1, further comprising:

Inserting said data of said one or more physical registers into said at least one register cache according to said potential significance (Kadambi: Column 4 lines 40-49)(Megiddo: Column 3 lines 35-46)(The combination of Kadambi and Megiddo results in the FBR algorithm maintaining a counter for all of the physical registers stored in the register pane. The potential significance of having a lower count value will mean that upon a replacement of a physical register within the register pane, the lowest count value will be used for the replacement.).

12. As per claim 3:

Kadambi, Megiddo, and Cherabuddi disclosed the method of claim 2, wherein said inserting said data is conditional on said potential significance being high (Kadambi: Column 4 lines 40-49)(Megiddo: Column 3 lines 35-46)(The combination of Kadambi and Megiddo results in the FBR algorithm maintaining a counter for all of the physical registers stored in the register pane. The potential significance of having a lower count value will mean that upon a replacement of a physical register within the register pane, the lowest count value will be used for the replacement. It would have been obvious to one of ordinary skill in the art that the counters could instead be started at the highest value and decremented. One of ordinary skill in the art at the time of the invention would have realized this would lead to a high counter value being used for the replacement instead of a low value.).

13. As per claim 4:

Kadambi, Megiddo, and Cherabuddi disclosed the method of claim 2, wherein said inserting said data is conditional on said potential significance being low (Kadambi: Column 4 lines 40-49)(Megiddo: Column 3 lines 35-46)(The combination of Kadambi and Megiddo results in the FBR algorithm maintaining a counter for all of the physical registers stored in the register pane. The potential significance of having a lower count value will mean that upon a replacement of a physical register within the register pane, the lowest count value will be used for the replacement.).

14. As per claim 5:

Kadambi, Megiddo, and Cherabuddi disclosed the method of claim 2, wherein said data is inserted into an empty slot in said at least one register cache (Kadambi: Figure 3 element 310, column 4 lines 36-39)(The physical register is written into an empty slot when there are empty slots available.).

15. As per claim 7:

Kadambi, Megiddo, and Cherabuddi disclosed the method of claim 1, said tracking one or more physical register references further comprising:

Associating at least one physical register identifier with said at least one instruction (Kadambi: Figure 1 elements 102 and 104, column 3 lines 6-33)(It's inherent that an instruction that contains operands will be associated with physical registers.);

Associating at least one counter with said physical register identifier (Megiddo: Column 3 lines 35-46)(A counter is associated with each physical register within the register pane.); and

Varying said at least one counter for each of said physical register references according to said at least one instruction (Megiddo: Column 3 lines 35-46)(The counter is incremented for physical register references not in the new section.).

16. As per claim 8:

Kadambi, Megiddo, and Cherabuddi disclosed the method of claim 7, wherein said at least one counter is incremented for each of said at least one physical register references (Megiddo: Column 3 lines 35-46)(The counter is incremented for physical register references not in the new section.).

17. As per claim 9:

Claim 9 essentially recites the same limitations of claim 1. Claim 9 additionally recites the following limitations:

Counter look-up table tracks references (Kadambi: Figure 1 element 102, column 3 lines 13-33)(Megiddo: Column 3 lines 35-46)(It would have been obvious to one of ordinary skill in the art that the counters for the replacement algorithm relating to the physical registers stored in the register pane could have been stored in a table.); and

One or more physical registers to store data associated with said at least one instruction (Kadambi: Figure 1 element 104, column 3 lines 6-12).

18. As per claim 10:

Claim 10 essentially recites the same limitations of claim 2. Therefore, claim 10 is rejected for the same reasons as claim 2.

19. As per claim 11:

Claim 11 essentially recites the same limitations of claim 3. Therefore, claim 11 is rejected for the same reasons as claim 3.

20. As per claim 12:

Claim 12 essentially recites the same limitations of claim 4. Therefore, claim 12 is rejected for the same reasons as claim 4.

21. As per claim 13:

Claim 13 essentially recites the same limitations of claim 5. Therefore, claim 13 is rejected for the same reasons as claim 5.

22. As per claim 15:

Claim 15 essentially recites the same limitations of claim 7. Therefore, claim 15 is rejected for the same reasons as claim 7.

23. As per claim 16:

Claim 16 essentially recites the same limitations of claim 8. Therefore, claim 16 is rejected for the same reasons as claim 8.

24. As per claim 17:

Claim 17 essentially recites the same limitations of claim 1. Claim 17 additionally recites the following limitations:

Counter look-up table tracks references (Kadambi: Figure 1 element 102, column 3 lines 13-33)(Megiddo: Column 3 lines 35-46)(It would have been obvious to one of ordinary skill in the art that the counters for the replacement algorithm relating to the physical registers stored in the register pane could have been stored in a table.);

An interface to couple said processor to input-output devices (Kadambi: Figure 1 element 114, column 2 lines 52-65)(The bus serves as an interface between the processor and the memory to transfer data between the two.); and

A data storage coupled to said interface to receive code from said processor (Kadambi: Figure 1 element 114, column 2 lines 52-65).

25. As per claim 18:

Claim 18 essentially recites the same limitations of claim 2. Therefore, claim 18 is rejected for the same reasons as claim 2.

26. As per claim 19:

Claim 19 essentially recites the same limitations of claim 3. Therefore, claim 19 is rejected for the same reasons as claim 3.

27. As per claim 20:

Claim 20 essentially recites the same limitations of claim 4. Therefore, claim 20 is rejected for the same reasons as claim 4.

28. As per claim 21:

Claim 21 essentially recites the same limitations of claim 5. Therefore, claim 21 is rejected for the same reasons as claim 5.

29. As per claim 23:

Claim 23 essentially recites the same limitations of claim 7. Therefore, claim 23 is rejected for the same reasons as claim 7.

30. As per claim 24:

Claim 24 essentially recites the same limitations of claim 8. Therefore, claim 24 is rejected for the same reasons as claim 8.

31. Claims 6, 14, and 22 are rejected under 35 U.S.C. §103(a) as being unpatentable over Kadambi et al. (U.S. 6,934,830), in view of Megiddo et al. (U.S. 6,996,676), in view of Cherabuddi (U.S. 6,263,416), further in view of Choquette (U.S. 6,088,784).

32. As per claim 6:

Kadambi, Megiddo, and Cherabuddi disclosed the method of claim 2, further comprising:

Selecting previous data from a slot in said at least one register cache according to the potential significance of said previous data (Kadambi: Column 4 lines 40-49)(Megiddo: Column 3 lines 35-46)(The combination of Kadambi and Megiddo results in the FBR algorithm maintaining a counter for all of the physical registers stored in the register pane. The potential significance of having a lower count value will mean that upon a replacement of a physical register within the register pane, the lowest count value will be used for the replacement.); and

Kadambi, Megiddo, and Cherabuddi failed to teach evicting said previous data from said slot in said at least one register cache prior to said inserting said data.

However, Choquette disclosed evicting said previous data from said slot in said at least one register cache prior to said inserting said data (Choquette: Figure 2 element 104, column 3 lines 56-64 and column 4 lines 25-31)(The combination of Choquette to

Kadambi results in all execution results only being written to the register pane. The results then stored in the register pane are selectively written back to the register file when needed. Thus, it's inherent that the data would have to be evicted from the register pane before it was inserted to avoid losing the data.).

The processor of Kadambi writes all execution results into both the register pane and the register file. While this is a simple policy of keeping the two memories synchronized, it's a very wasteful process in terms of power consumption. The processor of Choquette eliminates most of these writes by determining which execution results should be stored within the global bypass structure and which results should be written back to the register file. This process results in many fewer writes to the register file because the results in the global bypass will likely be used many times before needing to be written back. The advantage of saving power consumption would have motivated one of ordinary skill in the art at the time of the invention to implement the register pane of Kadambi with the ability to selectively write back instruction results. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the register pane that can write back instruction results selectively for the advantage of reduced power consumption.

33. As per claim 14:

Claim 14 essentially recites the same limitations of claim 6. Therefore, claim 14 is rejected for the same reasons as claim 6.

34. As per claim 22:

Claim 22 essentially recites the same limitations of claim 6. Therefore, claim 22 is rejected for the same reasons as claim 6.

Conclusion

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Nguyen et al. (U.S. 6,986,024), taught selecting physical register data from a temporary buffer or a register file.

Regev et al. (U.S. 6,934,797), taught using a least frequently used replacement method for a content addressable memory.

Rodriguez et al. (U.S. 6,823,428), taught preventing cache floods using a least frequently used replacement or least recently used algorithm.

Arlitt et al. (U.S. 6,272,598), taught using two different LFU algorithms for cache replacement.

Courtright, II et al. (U.S. 6,105,103), taught using a LRU or MFU algorithm for cache replacement.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacob Petranek whose telephone number is 571-272-5988. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jacob Petranek
Examiner
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